IN THE CLAIMS

A clean set of all pending claims is submitted, consolidating all previous versions of pending claims. If changes have been made to the previous version of the claims by the current response, the clean set is followed by a marked-up version indicating the changes made (see 37 CFR 1.121(c)(3)).

1. (AMENDED) An apparatus comprising:

a polarity switch comprising (i) a first memory cell connected to an input terminal of a first transmission gate and (ii) a second memory cell connected to an input terminal of a second transmission gate, wherein an input signal of said polarity switch is presented to a first control terminal of said first and said second transmission gates and an output of said polarity switch is configurable in response to contents of said first and second memory cells to present either (i) a signal that varies in response to said input signal or (ii) a predetermined logic level that is independent of said input signal.

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2. (AMENDED) The apparatus according to claim 1, wherein said first and second transmission gates further comprise a second control terminal configured to receive a complement of said input signal.

3. (AMENDED) The apparatus according to claim 1, wherein said first and second memory cells comprise a first configuration bit and a second configuration bit of said apparatus.

4. (AMENDED) The apparatus according to claim 1, wherein an output terminal of said first transmission gate and an output terminal of said second transmission gate are connected to said output of said polarity switch.

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5. (AMENDED) The apparatus according to claim 1, wherein said input signal comprises an input term and said output is configured to present a product term input.

6. (AMENDED) An apparatus comprising:

a first circuit configured to present a first value stored in a first memory cell to an input node in response to a first state of an input signal; and

a second circuit configured to present a second value stored in a second memory cell to said input node in response to a second state of said input signal, wherein said first and said second stored values are programmable during configuration of said apparatus.

7. (AMENDED) The apparatus according to claim 6, wherein said first and second circuits each comprise said first and second memory cells coupled to an input terminal of a first and a second transmission gates, respectively, and said input signal is coupled to a control terminal of said transmission gates.

8. The apparatus according to claim 7, wherein said transmission gates comprise a CMOS transistor pair.

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9. (AMENDED) The apparatus according to claim 7, wherein said first and second circuits further comprise a first and a second CMOS inverters coupling said first and second memory cells to said first and second transmission gates.

10. (AMENDED) The apparatus according to claim 7, wherein said output of said apparatus presents (i) a predetermined logic level when said memory cells of said first and said second circuits contain the same data and (ii) a signal that varies in response to said input signal when said memory cells contain different data.

11. The apparatus according to claim 10, wherein said data comprises configuration bits.

12. (AMENDED) The apparatus according to claim 7, wherein said memory cells are configured to source and sink a current.

13. The apparatus according to claim 6, wherein said apparatus comprises a product term input circuit of a programmable logic device.

14. An AND plane of a programmable logic device comprising one or more apparatus according to claim 6.

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15. (AMENDED) The apparatus according to claim 6, wherein said input signal comprises an input term.

16. (AMENDED) The apparatus according to claim 15, wherein said apparatus is programmable to present any of (i) said input term, (ii) a digital complement of said input term, and (iii) a predetermined logic level to said input node.

17. (AMENDED) The apparatus according to claim 16, wherein said predetermined logic level is selectable from a digital 0 and a digital 1.

18. (AMENDED) A method for providing a product term input of a programmable logic device comprising the steps of:

(A) presenting a first value stored in a first memory cell to an input node in response to a first state of an input signal; and

(B) presenting a second value stored in a second memory cell to said input node in response to a second state of said input signal, wherein said first and said second stored values are programmed during configuration of said programmable logic device.

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19. (AMENDED) The method according to claim 18, wherein said input signal comprises an input term of a logic block of said programmable logic device.

20. The method according to claim 18, further comprising the steps of:

(C) generating a first logic level at said input node in response to said first and said second stored values being programmed with a first value;

(D) generating a second logic level at said input node in response to said first and said second stored values being programmed with a second value;

(E) generating a signal at said input node that has a state similar to said control signal in response to said first

stored value being programmed with said first value and said second stored value being programmed with said second value; and

(F) generating a signal at said input node that has a state similar to a digital complement of said control signal in response to said first stored value being programmed with said second value and said second stored value being programmed with said first value.